ON-CHIP HOT SPOT COOLING: FORCASTS AND REALITY

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Abstract

The problem of suppression of local overheated areas (so-called “hot spots”) at the surface of modern microprocessor using miniature thermoelectric coolers (TECs) is studied with the goal to determine maximum attainable efficiency of this technology. Theoretical method of optimal thermal integrating of a micro TEC into a processor-to-heat sink interface is developed. The advantages and limitations of this approach are discussed.

Nomenclature

T_a	ambient temperature (K)
T_b	heat sink base temperature without TEC (K)
T_{b1}	heat sink base temperature with TEC activated (K)
R_h	heat sink thermal resistance (K/W)
Θ	overheat above heat sink base temperature (K)
T_p	hot spot peak temperature (K)
T_c	temperature at the TEC cold junctions (K)
T_h	temperature at the TEC hot junctions (K)
Q_c	heat flux at the TEC cold side (W)
Q_h	heat flux at the TEC hot side (W)
P	TEC input power (W)
COP	$=Q_c/P$ coefficient of performance
α	Seebeck coefficient (V/K)
κ	thermal conductivity (Wcm^{-1}K^{-1})
ρ	TE material electrical resistivity (Ωcm)
ρ_e	$=\rho(1+2R_c/\rho l)$
R_c	electrical contact resistance at the TEC junctions (Ωcm^2)
i	electrical current density (A/cm^2)
l	TE leg length (cm)
F_j	total TEC cold/hot junction area (cm^2)
F	$=F_j/\beta$ TEC substrate surface area (cm^2)
β	TE pellets packing density
R_s	$=\dfrac{\delta_s}{\kappa_s F}$ TEC substrate thermal resistance (K/W)
δ_s	substrate thickness (cm)
κ_s	substrate thermal conductivity (Wcm^{-1}K^{-1})

Introduction

Permanent increase in thermal dissipation of modern microprocessors becomes the dominant challenge in IC technology and this stimulates researchers to developing the most refined thermal solutions. The use of uniform chip cooling is a typical approach to the processor thermal management [1,2,3]. But aside from the distributed heat dissipation, one or more on-chip “hot spots” can exist in the processor area, which generates extremely intensive heat flux. Effective suppression of such sub-millimeter hot spots along with the whole chip moderate cooling seems to be a reasonable technique. The use of thermoelectric micro coolers for this purpose was considered recently by different scientific groups [4,5,6] with the conclusion that this novel technology can lead to the selective hot spots suppression what can contribute greatly to a processor operation life and efficiency. Just this circumstance encouraged us to make thorough analysis of this advanced thermal solution.

In this paper the results of detailed estimations are given concerning the attainable maximum efficiency of the cooling technique under discussion. The method of optimal thermal integrating of a micro TEC into a processor-to-heat sink interface is developed. A typical Intel processor is considered with powerful hot spot in the center of Si die. Prospects for the use of different TEC configurations are reviewed, including traditional bulk micro TECs and film-type micro coolers based on standard bismuth-tellurides and their nanostructured superlattices. The optimal TEC geometry and its operational mode are found providing minimal hot spot temperature. Some important factors which are neglected in other studies are taken into account what makes obtained results more realistic.

1. Processor with Integrated Micro-TEC

1.1 Chip package model

Figure 1 gives a schematic illustration of a chip package. A silicon die with a central hot spot at its active side is located at the copper heat spreader which is interfaced with a heat sink base. All parts are contacted through thermal interface materials (TIM1 and TIM2) insuring their efficient thermal connection. The TEC is accommodated in the square cavity made in the heat spreader and thin copper plate with a small tip at its top surface (so called “mini-contact” [4]) is attached to the TEC cold side to provide efficient thermal touch with the Si die through the TIM1 layer. The system parts geometry and material properties are given in the Table 1.

The heat generated in the active region of the die is modeled as a uniform heat flux of 1250 W/cm^2 on a 0.4x0.4 mm hot spot and a uniform heat flux of 70 W/cm^2 on the rest active surface of 11x13 mm silicon chip, the total heat dissipation being of 102 W.

The most important problem is to define such TEC configuration and its operating mode which would provide maximum hot spot suppression. Several factors make this problem unusually complicated. First of all, the TEC hot side turns to be thermally connected with its cold area through surrounding parts, so one never knows what actual heat load is at the TEC cold side. Besides, the TEC itself is an energy consumer, hence its application increases overall heat load to the heat sink, what can lead to additional Si die overheat instead of its cooling.

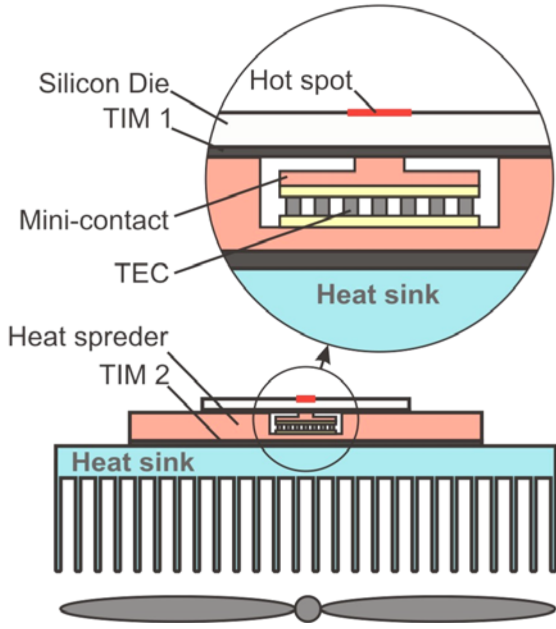

Figure 1 Scheme of a chip package with integrated micro-cooler.

Table 1 System geometry and thermal parameters

Mechanical Part	Geometry (mm)	Material Physical properties
Hot spot	0.4x0.4	-
Die	11x13x0.5	Silicon κ=110 W/m/K
TIM1	11x13x0.03	In solder κ=75 W/m/K
Heat spreader	31x31x1.5	Copper κ =360 W/m/K
TIM2	31x31x0.05	Arcticsilver [7] κ= 8.9 W/m/K
Heat sink base	50x50x5	Aluminium κ =180 W/m/K
Substrates: - thickness - surface area	0.2 mm To be varied	AlN ceramic κ=180 W/m/K
TE pellets: - cross-section - pitch - packing density - height	0.4x0.4 mm 0.6 mm 0.444 To be varied	Bismuth Telluride κ =1.4 W/m/K α=200 μV/K $\rho=10^{-3}$ Ωcm
Mini-contact tip - cross-section - height Mini-contact base - cross-section - height	 To be varied 0.05 mm To be varied 0.4 mm	Copper κ =360 W/m/K

In particular, it may take place when the heat sink is not enough efficient or the TEC is not subjected to the demand of minimum power consumption. This is why the substantiated choice of a TEC configuration and its operating mode becomes of primary importance.

We will assume that the side surfaces of the structure are insulated adiabatically. Hence, all the heat generated in the structure is to be transferred through the finned heat sink to ambient by forced convection. In this model we will ignore the details of the heat sink construction. Instead, we suppose that the heat sink base is maintained at the uniform temperature T_b. This temperature will be taken as a reference point for counting out the field of excess temperatures in different areas of the processor. We will assume in our calculations that with the TEC switched off T_b value is of 100°C what leads to critical overheat in the hot spot area. With the heat load to the heat sink of 102 W and ambient at 25°C, this corresponds to overall heat sink thermal resistance of 0.735 K/W. This quantity will be regarded henceforth as a practical minimum for R_h value matched with definite restrictions imposed on the heat sink dimensions.

The TEC being switched on, an additional heat equal to the TEC input power P arises. As a result, the heat sink base temperature T_b will be increased by R_hP quantity and the heat spreader temperature will raise simultaneously what diminishs efficiency of a TEC application. These considerations are taken ito account in this study.

1.2 Chip package thermal characterization

Generally, three parameters are necessary to fully identify TEC configuration. These are a TEC cold side and hot side temperatures T_c, T_h and necessary cooling power Q_c. No one of these parameters is known beforehand in our case. So the problem is to develop adequate method of their determination. The key idea used in this study was to find dependences of the hot spot peak overheat Θ_p and corresponding excessive temperatures at the TEC outer boundaries Θ_c and Θ_h on heat fluxes Q_c and Q_h at these boundaries. With this goal, the system model was considered in which a TEC operation was imitated by uniform heat fluxes Q_c and Q_h at its interfaces with adjacent structure parts (Figure 2).

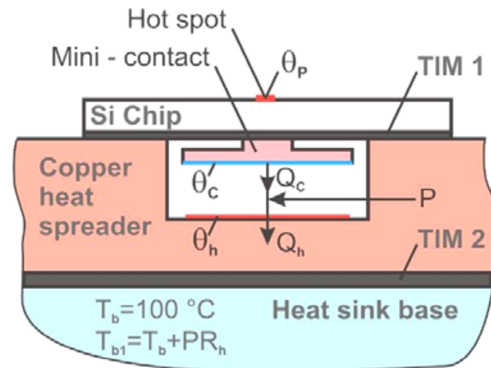

Figure 2 Scheme of the TEC equivalent replacement

Numerical method analogous to that used in [4,5] was applied for calculating 3-dimensional temperature distribution in the processor structure. Total 7 TEC dimensional types with footprints F from 2.4x2.4 mm to 7.2x7.2 mm were chosen for simulation (Table 2). Different mini-contact tip dimensions in the range from 1x1 to 2.5x2.5 mm were tried with each TEC option to achieve the best cooling effect. In all cases the clearance of 0.1 mm was kept between the TEC side surfaces and cavity walls. As the first step, Q_h values were accepted to be of $2Q_c$ what corresponds to the TEC COP=1.

Table 2 Dimensional details of the used model (mm)

TEC option No.	Footprint F	Junctions area F_j	Cavity size
1	2.4x2.4	2.56	2.6x2.6
2	3.0x3.0	4	3.2x3.2
3	3.6x3.6	5.76	3.8x3.8
4	4.2x4.2	7.84	4.4x4.4
5	4.8x4.8	10.24	5.x5
6	6x6	16	6.2x6.2
7	7.2x7.2	23.04	7.4x7.4

Figures 3 and 4 show results of calculations for the TEC option no. 4 (F=4.2x4.2 mm) with tip size of 1.4 mm. It is seen that the sought dependences can be treated as linear having the form:

$$\theta_p = a_0 + a_1 Q_c$$
$$\theta_c = b_0 + b_1 Q_c \qquad (1)$$
$$\theta_h = c_0 + c_1 Q_h$$

Corresponding coefficients are given in the Table 3. Similar dependences for all the TEC options coupled with different mini-contacts are defined and are found to be in excellent agreement with the linear form.

Table 3 Coefficients in the dependences (1) (4.2x4.2 mm TEC, tip size of 1.4 mm).

a_0	a_1	b_0	b_1	c_0	c_1
58.433	-3.916	35.5089	-5.3378	2.69	0.1802

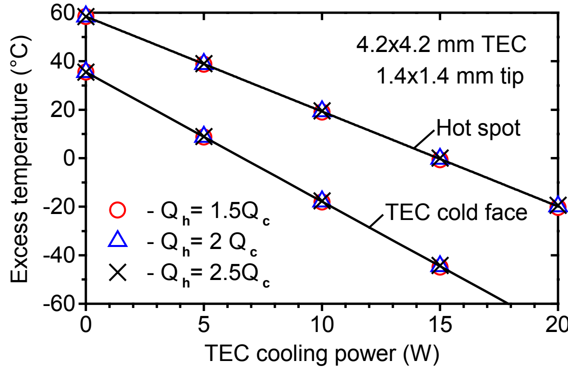

Figure 3 Dependence of hot-spot peak overheat and mean integral excess temperature at the TEC cold footprint on heat flux absorbed.

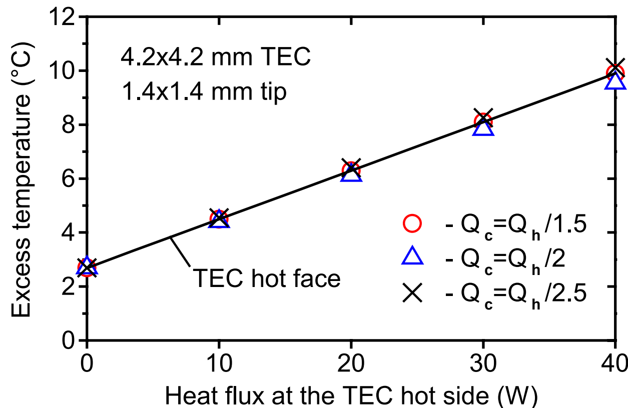

Figure 4 Dependence of the mean integral excess temperature at the TEC hot footprint on heat flux.

The following question is a crucial one for proposed method applicability: do the obtained coefficients remain unchanged when TEC COP deviates considerably from the unit or they are dependent on TEC efficiency? To clear this question, the estimations were undertaken in which the aforesaid coefficients were recalculated with Q_h values defined as $1.5Q_c$ and $2.5Q_c$ what covers entire region of COP practical variation. It is seen (Figure 3) that drastic vriation of Q_h value does not affect practically excessive temperatures Θ_p and Θ_c and, just the same, considerable changes in Qc value exert negligible influence on the $\Theta_h(Q_h)$ dependence (Figure 4). This means that the relations (1) have a content of generalized chip package thermal characteristics. They are independent on the actual temperature of the heat sink base, are not affected whith a TEC efficiensy variation and therefore can serve as a basis for optimal integration of a TEC into the chip package. Once again, it has to be noted that the system (1) gives the field of excess temperatures over heat sink real temperature T_{b1}, which do depends on the heat flux Q_h in accordance with the formula T_{b1}=T_b+R_h(Q_h-Q_c).

1.3 The TEC analytical model

The analytical model of the TEC integrated into the chip package can be given by following system of linear equations:

$$Q_c = F_j\left(\alpha i T_c - \frac{1}{2}i^2\rho_e l - \frac{\kappa}{l}(T_h - T_c)\right)$$
$$Q_h = F_j\left(\alpha i T_h + \frac{1}{2}i^2\rho_e l - \frac{\kappa}{l}(T_h - T_c)\right)$$
$$T_c = T_{b1} + \theta_c - Q_c R_s \qquad (2)$$
$$T_p = T_{b1} + \theta_p$$
$$T_h = T_{b1} + \theta_h + Q_h R_s$$
$$T_{b1} = T_b + (Q_h - Q_c)R_h$$

The system (2) includes heat balans equations at the TEC cold and hot junctions coupled with relations for tmperature drop at the TEC substrates. The last equation in the system reflects an additional overheating of the heat sink base caused by the supplimentary TEC input power, an unfavourable effect which is missing in some other studies.

1.4 Models Matching

Equations (2) together with the relations (1) form the clozed system of 9 linear equations regarding to 9 unknown variables T_p, T_c, T_h, T_{b1}, Θ_p, Θ_c, Θ_h, Q_c, Q_h,. We will consider F_j, l and i as independent variables. For any given set of these quantities the system has unique solution. Hence, here is the case of the implicitly defined $T_p(F_j,l,i)$ function. We will use F_j, l and i parameters to control hot spot overheat with the objective to find such TEC configuration and its operating mode which provide minimum hot spot peak temperature T_p=min$T_p(F_j,l,i)$. The problem is solved numerically using proposed thermal model of the processor. Various TEC total junction areas F_j were considered and for each F_j value the optimal TE pellet height l=l_0 and corresponding optimal current

density $i=i_0$ were defined using standard program of the two-variable function $T_p(l,i)$ minimization. This procedure was repeated for different mini-contact tip dimensions to find its optimal configuration resulting in maximum hot spot temperature suppression. Currently available R_c value of 10^{-6} Ωcm^2 was used in our calculations and effect of its reduction to 10^{-7} Ωcm^2 was also studied. Finally, the idealized case of $R_c=0$ was reviewed to find the theoretical limit for the efficiency of considered technology.

2. Results and Discussion

2.1 Optimal TEC configuration

Results of estimations are given at the Figures 5 to 8. Figure 5 shows the dependence of the hot spot peak temperaure on the TEC total junctions area for different R_c values. Each point at the figure is obtaind as a result of optimization of TE leg length, current dencitiy and mini-contact tip size. Corresponding optimal values are given in the Table 4.

Horizontal line at the Figure 5 corresponds to the hot spot temperature of 131.6°C for the case of solid heat spreader with no TEC integrated. From now onwards we will take this very temperature as a reference point when estimating hot spot suppression.

The best result is obtained for the TECs with the total junction area in the range from 7 to 9 mm^2. These are options 4 and 5 which relate to the TECs with 4.2x4.2 and 4.8x4.8 mm substrates correspondingly. It is seen that with $R_c=10^{-6}$ Ωcm^2 one can await the hot spot suppression of the order of 9°C only. With R_c reduction to 10^{-7} Ωcm^2 the attainable effect can be raised to 15.6°C and this looks like a practical limit for this tecnology. No farther progress is available because even for hypothetical case with $R_c=0$ an additional hot spot suppression does not exceed 1°C.

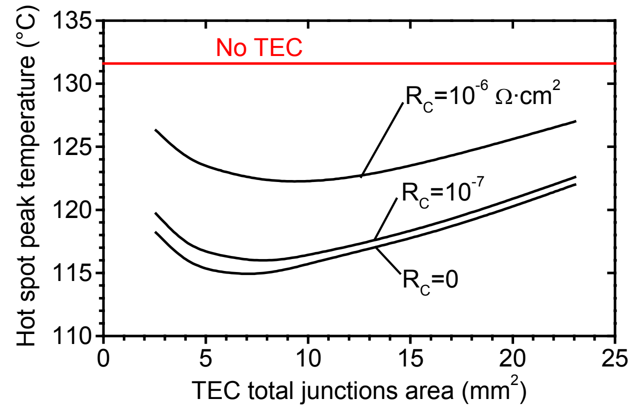

Figure 5 Dependence of hot spot peak temperaure on the TEC total junctions area. TE leg length, current density and mini-contact tip dimesions are optimized for each point.

Table 4 Optimal parameters for the TECs with different footprints (TECs dimensions are accordingly to the Table 2).

TEC option No.*	Optimal tip size (mm)	Optimized TEC parameters				Minimal T_p value (°C)	Hot spot suppression (°C)
		l (μm)	i (A/cm^2)	Q_c (W)	P (W)		
$\boldsymbol{R_c=10^{-6}}$ Ωcm^2							
1	1x1	28	7263	6.62	7.33	126.3	5.3
2	1.2x1.2	33	6360	8.77	9.97	124.3	7.3
3	1.3x1.3	41	5459	10.41	12.38	123.1	8.5
4	1.4x1.4	48	4774	11.96	14.64	122.3	9.3
5	1.5x1.5	56	4192	13.42	16.6	122.3	9.3
6	1.7x1.7	71	3312	16.3	19.9	123.9	7.7
7	1.9x1.9	86	2699	19.23	22.44	127	4.6
$\boldsymbol{R_c=10^{-7}}$ Ωcm^2							
1	1.1x1.1	18	13449	10.78	11.97	119.7	11.9
2	1.3x1.3	22	10787	10.98	14.54	117.5	14.1
3	1.5x1,5	27	8824	14.52	17.72	116.4	15.2
4	1.6x1.6	34	7226	15.85	19.87	116.0	15.6
5	1.8x1.8	39	6168	17.79	21.69	116.5	15.1
6	1.9x1.9	55	4402	19.58	24.29	118.8	12.8
7	2.1x2.1	69	3400	22.2	26.14	122.6	9

This means that the thermal resistances in the structure become predominant. Another disadvantage is the fact that optimal TE pellet heights lay in the region of several tens of micrones what is difficult to implement using bulk technology or thin-film technique as well.

It has to be noted that the results obtained do not correlate in details with the conclusions in the paper [4]. Though initial data for estimations are rather similar, the optimal TEC configuration found in this study is shifted to considerably greater dimensions and much higher input power.

Figure 6 shows temperature profiles at the active face of the silicon chip. If the heat flux of 70 W/cm^2 is dissipated uniformly in the chip surface and there is no hot spot and no TEC, the peack chip temperature is of 109°C. However when 0.4x0.4 mm hot spot with heat flux of 1250 W/cm^2 is activated, the peak chip temperature increases to 131.6°C. With the optimized TEC (option 4, $R_c=10^{-7}$ Ωcm^2) integrated into the heat spreader the temperature profile changes fundamentally possessing “W” shaped form with about 16°C reduction in the hot spot temperature and this effect is accompanied

with sharp temperature lowering around the hot spot area and its rising over the "no TEC" level at the chip distant area due to additional heat load equivalent to the TEC power.

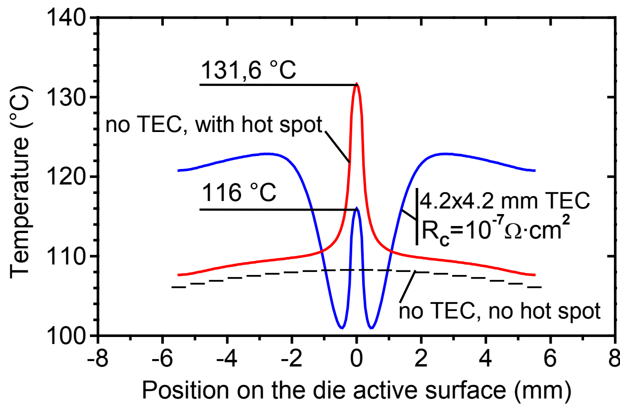

Figure 6 Temperature profile at the silicon chip surface.

2.2 Influence of the deviation from optimal parameters

As the practical implementation of the found optimal design can turn to be problematic, it would be of great interest to find in what degree the deviation from the TEC optimal parameters will affect its ability for hot spot suppression. In our farther calculations the optimal TEC model according to the item 4 (Table 4) will be considered as a reference one.

Effect of input power. Figure 7 shows hot spot temperature variation with TEC input power. It is seen that with the TEC switched off, the hot spot temperature becomes of 140°C what is 9°C higher than that for the case without TEC integrated. The power of near 2 W is necessary to compensate this unfavorable effect of the inactive TEC presence. With the TEC farther activation the hot spot temperature reduces and reaches defined minimums in the power range from 10 to 20 W.

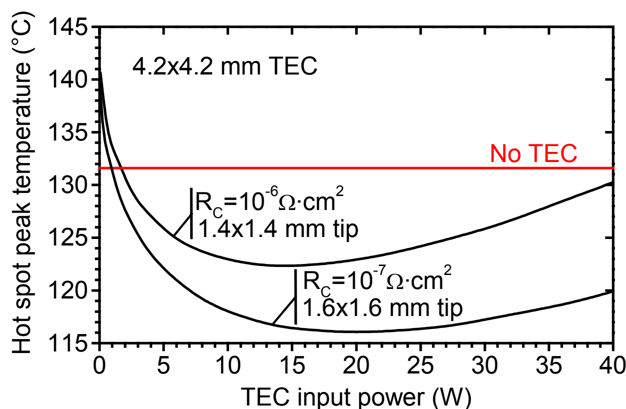

Figure 7 Dependence of hot spot peak temperaure on TEC input power (optimal TEC: Table 4, option 4).

Effect of TE pellet height. Figure 8 shows dependence of hot spot cooling on the TE pellet height. The optimal l values lay in the region from 35 to 50 microns and deviation from this region both to the left and to the right greatly affects hot spot cooling performance. It is seen also that bulk TECs with TE pellet heights over 0.18 mm are not applicable.

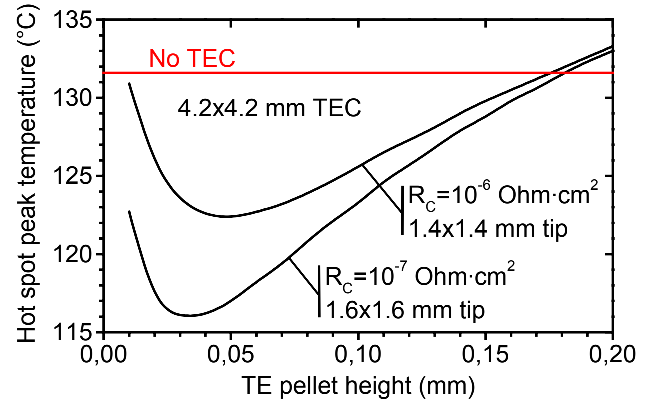

Figure 7 Dependence of hot spot temperature on TE leg height (current density is optimized for each l value).

Effect of the mini-contact tip dimensions. Mini-contact tip at the TEC-to-chip interface allows minimizing deleterious temperature drop at the TEC cold side. When its dimensions reduce, the heat gain to the TEC cold side reduces but thermal resistance of the mini-contact increases simultaneously. These two contradictive factors cause existence of optimal mini-contact size. For the device under consideration these optimums are found to be in the range from 1.4x1.4 to 1.6x1.6 mm (Figure 8). It is seen that expansion of this region to the boundaries 1x1 to 2x2 mm leads to 5°C loss in hot spot suppression what is over 30% of the disposable value.

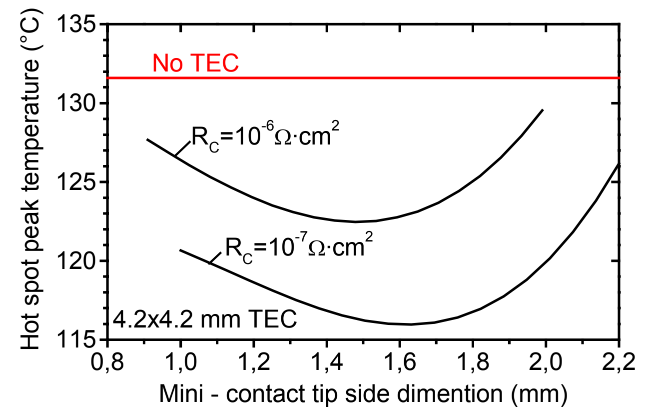

Figure 8 Effect of deviation of mini-contact tip dimensions from optimum (TE pellet height and electrical current are optimized at each point).

3. Further prospects

In this study, TE materials with z-factor of $3 \cdot 10^{-3}K^{-1}$, peculiar to modern bulk thermoelectrics, were considered and their potential for hot spot cooling is estimated with R_c value supposed to be lowered down to $10^{-7}\Omega cm^2$. It has to be noted, that with such parameters a TEC should give theoretically ΔT_{max} of 72°C even with TE legs as short as 20 μm. As this is not justified yet practically, the obtained limitations for on-chip hot spot cooling of about 10°C look like well-grounded for the state-of-the-art technology which provides R_c value at the level of $10^{-6}\Omega cm^2$.

Definite hopes are pinned today on the nanostructured TE materials which promise a fundamental improvement in micro TECs performance and technology. Venkatasubramanian *et al* [8] reported recently zT of 2.4 in p-Bi_2Te_3/Sb_2Te_3–based superlettices what can give a real breakthrough in the field of thermoelectric materials and, what is especially important, this achievement is now accompanied with considerable progress in the field of microcooler technology due to involvement of advanced methods of nano and micro electronics [9,10]. But as a matter of fact, no measured ΔT_{max} values approaching to 70°C at room temperature are still reported for such microdevices what proves the deteriorative influence of the thermal and electrical contact resistances. Hence, further prospects depend on what will be done to practically improve the micro TEC efficiency on the device level.

Conclusions

Performance of micro TECs in on-chip hot spot cooling application is greatly affected with electrical and thermal contact resistances. With the state-of-the-art thermoelectric technology, which provides electrical contact resistance at the level of 10^{-6} Ωcm^2, hot spot cooling of 10°C only can be awaited. With $R_c=10^{-7}\Omega cm^2$ this quantity can be enlarged to 15°C.

The optimal TE leg lengths for the TECs integrated in the chip package lay in the region of several tens of microns which is the most problematic to implement both with bulk and thin-film technology.

Bulk TECs with TE pellet height over 0.18 mm are unfit for hot spot cooling.

In view of these limitations, the use of the micro TECs is justified in only case, when on-chip thermal problem can not be solved by direct improvement in the heat sink performance.

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